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FORM PTO-1390 (REV. 12-2001)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER 18036-24199	
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371				U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	
				10/031672	
INTERNATIONAL APPLICATION NO. PCT/US00/19608		INTERNATIONAL FILING DATE 18 July 2000		PRIORITY DATE CLAIMED 19 July 1999	
TITLE OF INVENTION HIGH PERFORMANCE CLOCK-POWERED LOGIC					
APPLICANT(S) FOR DO/EO/US William C. Athas; Nestor Tzartzanis; Lena Peterson; Weihua Mao					
Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:					
<ol style="list-style-type: none">1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.3. <input type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.4. <input type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31).5. <input checked="" type="checkbox"/> A copy of the International Application as filed (35 U.S.C. 371(c)(2))<ol style="list-style-type: none">a. <input checked="" type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau).b. <input checked="" type="checkbox"/> has been communicated by the International Bureau.c. <input checked="" type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).6. <input type="checkbox"/> An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).<ol style="list-style-type: none">a. <input type="checkbox"/> is attached hereto.b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4).7. <input checked="" type="checkbox"/> Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))<ol style="list-style-type: none">a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau).b. <input type="checkbox"/> have been communicated by the International Bureau.c. <input checked="" type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.d. <input type="checkbox"/> have not been made and will not be made.8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).9. <input checked="" type="checkbox"/> An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)). Unexecuted10. <input type="checkbox"/> An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).					
Items 11 to 20 below concern document(s) or information included:					
<ol style="list-style-type: none">11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 CFR 1.97 and 1.98.12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.13. <input type="checkbox"/> A FIRST preliminary amendment.14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.15. <input type="checkbox"/> A substitute specification.16. <input type="checkbox"/> A change of power of attorney and/or address letter.17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.18. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4).19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).20. <input checked="" type="checkbox"/> Other items or information: Original Power of Attorney					

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U.S. APPLICATION NO. <u>10/031672</u> INTERNATIONAL APPLICATION NO. <u>PCT/US00/19608</u>				ATTORNEY'S DOCKET NUMBER <u>18036-24199</u>	
<div>21. <input checked="" type="checkbox"/> The following fees are submitted: BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. \$1040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO \$890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO \$740.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) \$710.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) \$100.00 ENTER APPROPRIATE BASIC FEE AMOUNT =</div>				CALCULATIONS PTO USE ONLY	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input checked="" type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				\$ 130.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	\$	
Total claims	41 - 20 =	21	x \$18.00	\$ 168.00	
Independent claims	4 - 3 =	1	x \$84.00	\$ 84.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ \$280.00	\$	
TOTAL OF ABOVE CALCULATIONS =				\$ 1092.00	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				\$	
SUBTOTAL =				\$ 1092.00	
Processing fee of \$130.00 for furnishing the English translation later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				\$	
TOTAL NATIONAL FEE =				\$ 1092.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property +				\$	
TOTAL FEES ENCLOSED =				\$ 1092.00	
				Amount to be refunded:	\$
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a. <input checked="" type="checkbox"/> A check in the amount of \$ <u>1092.00</u> to cover the above fees is enclosed.					
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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.					
SEND ALL CORRESPONDENCE TO: MARC E. BROWN, ESQ. OPPENHEIMER WOLFF & DONNELLY LLP 2029 CENTURY PARK EAST, SUITE 3800 LOS ANGELES, CA 90067 PHONE: (310) 788-5032 FAX: (310) 788-5100 E-MAIL: mbrown@oppenheimer.com					
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				REGISTRATION NUMBER	

HIGH-PERFORMANCE CLOCK-POWERED LOGIC

Government License Rights

The invention was made with government support under DARPA Contract Nos. DAAL 01-95-K3528 and DABT63-96-C-0001. The government has certain rights in the
5 invention.

Cross-Reference to Related Applications

This application claims the benefit of the filing date of U.S. Provisional Application No. 60/144,520, entitled "High-Performance Clock-powered Logic," filed July 19, 1999, and U.S. Provisional Application No. 60/174,509 entitled "A Low-Power
10 SRAM With Resonantly Powered Data, Address, Word and Bit Lines," filed January 5, 2000, the contents of both of which are incorporated herein by reference.

Background of Invention

Field of the Invention

This invention relates to digital systems and, more particularly, to digital systems
15 that are driven by clock-powered logic, including adiabatic signals.

Description of Related Art

Digital systems include signal lines that carry digital signals, including data lines, address lines and control lines.

In many instances, these signal lines are much longer than the distances between
20 the integrated circuitry components. Such long signal lines are commonly used to connect the various subsystems in an integrated circuit, as well as the pixels in an LCD display.

One of the primary problems with long signal lines is the substantial capacitance which they impose. As is well known, the presence of this substantial capacitance causes
25 a corresponding substantial loss in energy while the signal lines are being driven between one logic state and another, such as commonly occurs during the serial delivery of digital data over the signal lines.

One attempt to minimize these energy losses is to use what has become known as a "clocked buffer." In a typical digital system, the digital signal powers one end of a signal line by controlling switches that switch the end of the signal line between the supply voltage (typically logic "1") and ground (typically logic "0"). With a clocked
5 buffer, on the other hand, the digital signal is instead used to control the delivery of a clock signal into the input of the signal line.

If this clock signal rises and falls slowly, energy will be saved, particularly when energy stored in the capacitance of the signal lines is returned to a temporary storage device for re-use during the next clock cycle. The use of a slowly rising and falling
10 signal to power a digital system has become known as adiabatic charging and discharging. Examples of such signals are described in U.S. Patents 5,559,478 and 5,473,526.

Unfortunately, the use of clocked buffers to power logic has, in the past, had some drawbacks.

15 First, the circuitry usually requires the voltage of the clock signal to exceed the supply voltage, i.e., for the clock signal to run "hot." This may stress certain digital devices by forcing them to run at voltage levels beyond the levels for which they were designed. The excessive voltages, moreover, tend to offset the energy savings realized from the clock-powered approach, since energy loss increases as the square of the
20 voltage increase.

A second problem with existing clock-powered logic is that it often reduces the speed at which the logic circuitry can be clocked. Generally, the existing clock-powered logic systems require the logic circuitry to process the incoming digital signals and to generate an appropriate output signal within no more than one-half of the period of the
25 clock signal and, in many cases, on even a faster basis. This increases the required speed of the logic circuitry or, in the alternative, reduces the maximum speed of the clock signal.

Solutions to the problems of excessive clock signal voltage and insufficient processing time, moreover, have usually worked against one another. One way to reduce
30 the adverse consequences of "hot clocks" is to reduce the voltage of these clocks. Reducing clock signal voltage, however, usually reduces processing speed, thereby requiring clock signal speed to be even further reduced. Conversely, the speed at which the logic processes its signals can usually be increased by increasing the voltage of the

clock signal. Unfortunately, this increases concerns over device stress and energy dissipation.

In short, there continues to be a need in the art for clock-powered logic that maximizes the conservation of energy without stressing devices, nor slowing system performance.

Summary of Invention

One object of the invention is to obviate these as well as other problems in the prior art.

Another object of the invention is to reduce energy consumption in digital systems.

A still further object of the invention is to increase the speed at which digital systems can operate.

A still further object of the invention is to reduce stress on digital circuitry components.

A still further object of the invention is to provide more time for digital logic circuitry to process signals, without slowing clock signal speed.

A still further object of the invention is to reduce the voltage of clock-powered logic.

These, as well as still further features, objects and benefits of the invention, are achieved through the use of various circuitry components, configurations and processing methods.

In one embodiment of the invention, a signal level booster has an input configured to be in communication with a signal that is reflective of the input digital signal. The booster also has an output that is reflective of the input to the signal level booster, but of greater magnitude.

A first latch has an input in communication with the output of the signal level booster. It is configured to be toggled by the output of the signal level booster and by a first clock signal. The first latch also has an output.

Digital logic has an input in communication with a signal that is reflective of the output of the first latch. The digital logic also has an output.

A second latch has an input in communication with the output of the digital logic. It is configured to be toggled by the output of the digital logic and by the first clock signal. The second latch has an output configured to deliver the output digital signal.

In one embodiment, a jam latch functions as the signal level booster and as the first latch. The second latch may also include an n-latch.

In one embodiment, the input digital signal and the output digital signal are each a single signal. In another embodiment, they are a complementary pair of signals.

In a still further embodiment, a clocked buffer is configured to be powered by a second clock signal that is complementary to and substantially non-overlapping with the first clock signal. The clocked buffer has an input configured to be in communication with the input digital signal. It also has an output in communication with the signal level booster.

Preferably, the second clock signal is an adiabatic signal. The adiabatic signal may include blips, a staircase signal or a ramp signal.

In a still further embodiment, a third latch is provided having an input in communication with the output of the first latch. The third latch is configured to be toggled by the output of the first latch and by the second clock signal. The third latch has an output in communication with the input to the digital logic. The third latch may include an n-latch.

The invention also includes methods of signal processing, including methods implemented by the circuitry discussed above.

The invention also includes other structures, methods, features and benefits, as will now become clear from a review of the following detailed description of the preferred embodiments and the attached drawings and claims.

Brief Description of Drawings

FIG. 1 is a block diagram of the architecture of a typical prior art clock-powered logic system.

FIG. 2 is a block diagram of the prior art energy recovery latch shown in FIG. 1.

FIG. 3. is a graph of the prior art complementary and substantially non-overlapping clock signals generated by the clock driver shown in FIG. 1.

FIG. 4 is a typical prior art circuit for the prior art clocked buffer shown in FIG. 2.

FIG. 5 is a graph of two of the signals that are typically generated by the prior art circuit shown in FIG. 4.

FIG. 6 is a diagram of some of the typical prior art components relating to the prior art digital logic shown in FIG. 1.

5 FIGS. 7 (a) – (c) are graphs of other typical prior art adiabatic signals that may be used in the prior art clock-powered logic shown in FIG. 1.

FIG. 8 is a block diagram of one embodiment of the invention.

FIG. 9 is one embodiment of a circuit of the invention that is shown in FIG. 8.

10 FIG. 10 is a block diagram of another embodiment of the invention using complementary input signals, but only a single latch between the clocked buffer and the digital logic.

FIG. 11 is a circuit of one embodiment of the level booster and latch shown in FIG. 10.

15 FIG. 12 is a block diagram of another embodiment of the invention that does not use two latches between the clocked buffer and the digital logic, nor complementary digital input signals.

Detailed Description of Preferred Embodiments

FIG. 1 is a block diagram of the architecture of a typical prior art clock-powered logic system.

20 As shown in FIG. 1, the digital signal to be processed, D_{in} in this example, is delivered to an energy recovery latch 1. The output of the energy recovery latch 1 is delivered to digital logic 3.

Digital logic 3 represents the digital logic that processes the signal received from the energy recovery latch 1, typically over a long signal line, such as signal line 4.

25 The output of the digital logic 3 is delivered to a second energy recovery latch 5. The output of the second energy recovery latch 5 is delivered to a second set of digital logic 7. This architecture repeats until the digital signal, D_{in} , is processed by all of the needed digital logic, leading to the generation of the output digital signal, D_{out} in this example. The energy recovery latches, including latches 1 and 5, operate under the
30 control of a clock driver 9.

FIG. 2 is a block diagram of the prior art energy recovery latch 1 shown in FIG. 1. As shown in FIG. 2, the prior art energy recovery latch 1 includes a latch 21 and a clocked buffer 23. A capacitor 25 is included to illustrate the capacitance that the signal line 4 imposes.

5 FIG. 3 is a graph of the complementary and substantially non-overlapping clock signals ϕ_A and ϕ_D generated by the prior art clock driver 9 shown in FIG. 1, the partial routing of which are shown in FIG. 2. The phrase "substantially non-overlapping" is used to indicate that a small degree of overlap is permissible.

10 FIG. 4 is a typical prior art circuit of the prior art clocked buffer 23 shown in FIG. 2. As shown in FIG. 4, the latched data, illustrated in Fig. 4 as $\overline{D_{inL}}$, is delivered to an inverter 41 and then to an electronic switch 43. V_{iso} represents a reference voltage which, as will soon be seen, is quite high.

15 In operation, D_{out} reflects the complementary clock signal phase ϕ_B when $\overline{D_{inL}}$ is low. This occurs through the operation of electronic switch 43, as well as electronic switches 45 and 47. In essence, the clock signal ϕ_B becomes buffered and metered by the data signal.

20 FIG. 5 is a graph of two of the signals that are typically generated by the prior art circuit shown in FIG. 4, namely D_{out} and D_{bn} . As seen in FIG. 5, D_{bn} must rise above the level of D_{out} during the cycle. Because D_{out} is typically at the supply level, this usually means that D_{bn} is above the supply level and, as a consequence, that ϕ_B must be above the supply level.

25 This excessive voltage in ϕ_B is known as a "hot clock" and, as explained above, is undesirable. It potentially places stress on the components in the system and increases energy dissipation. Even greater stress is placed on the devices connected to D_{bn} .

30 FIG. 6 is a diagram of some of the typical prior art components relating to the prior art digital logic shown in FIG. 1. Clocked buffer 61 is just one of many clocked buffers that are used in the system, such as the one illustrated in FIG. 2. Electronic switches 63 and 65 form a latch that is controlled by the output of the clocked buffer 61 and the clocked signal ϕ_A . The output of this latch is inverted by an inverter 67 and delivered to digital logic circuitry 69. In order to preserve the state of the digital logic circuitry 69 after processing input data, the output of the digital logic circuitry 69 is

delivered to an electronic switch 71 and to an inverting buffer 73. The output of the inverting buffer 73 is then again delivered to a clocked buffer 75 to generate D_{out} .

In order to ensure the proper functioning of the inverting buffer 73, the input to the inverting buffer 73 must be at near-supply level during its logic "1" state. In turn, this
5 requires the voltage of the clock signal ϕ_A to be above the supply level, just like with ϕ_B . This again raises concerns over circuitry stress and increases energy dissipation.

As explained above, another problem with the clock-powered logic in the prior art is that the digital logic circuitry must operate very quickly. More specifically, the digital logic 69 must operate fast enough to generate an output by the time its input
10 signal is removed. In the typical prior art circuit, the input signal to the digital logic 69 begins on the rising edge of clock signal ϕ_B and ends on the falling edge of clock signal ϕ_B . In order to generate a stable output during this interim, the digital logic 69 must either be very fast or the clock signal ϕ_B must be very slow. Neither approach is desirable.

15 To maximize energy conservation, the clocks should rise and fall as slowly as possible. Signals with slow rising and falling edges have become known as adiabatic signals. Thus far, one form of slowly rising and falling edges has been shown in FIG. 3. Another form is a blip signal, as shown in FIG. 7(a). Another form is a staircase signal, as shown in FIG. 7(b). A still further form is a ramp signal, as shown in Fig. 7(c). A circuit
20 for generating the blip signal shown in FIG. 7(a) is disclosed in U.S. Patent 5,559,478. A circuit for generating the staircase signal shown in FIG. 7(b) is shown in U.S. Patent 5,473,526. The content of both of these patents is incorporated herein by reference.

FIG. 8 is a block diagram of one embodiment of the invention. As will soon be seen, FIG. 8 represents clock-powered logic that utilizes a clock signal that is below the
25 supply voltage, without sacrificing speed. Further, the system shown in FIG. 8 allows the clock signal speed to be faster, without increasing the speed of the logic.

As shown in FIG. 8, a digital signal, such as D_{in} , is used to control a clocked buffer 101 that operates under the control of a clock signal ϕ_B . The clocked buffer 101 is the same as the clocked buffers shown in the prior art, except that it produces a clocked
30 signal of lower voltage and does not require a "hot clock."

A level booster 103 receives the clocked signal from the clocked buffer 101 and boosts its level. The output of the level booster 103 is delivered to a latch 105 that

operates under the control of the clock signal ϕ_A . The output of the latch **105** is delivered to a second latch **107** that operates under the control of the clock signal ϕ_B . The output of the latch **107** is delivered to digital logic **109**. Digital logic **109** is any form of digital logic, including data processing circuitry, memory, control circuitry, and addressing circuitry.

The output of the digital logic **109** is delivered to a third latch **111** that operates under the control of the clock signal ϕ_A . The output of the latch **111** represents the final processed digital signal D_{out} .

The data signals, D_{in} and D_{out} , are merely representative of the types of digital signals that the invention can process. The invention is equally useful in connection with all other types of digital signals, such as digital signals representing addresses or control.

The clock signals ϕ_A and ϕ_B are preferably the same type of complementary and substantially non-overlapping clock signals that were discussed above in connection with the prior art, namely the trapezoid signals shown in FIG. 3, or the blips, staircase or ramp signals shown in FIG. 7. Other adiabatic wave shapes can also be used. Indeed, the invention is also applicable to fast-rising, non-adiabatic signals, although it is anticipated that there would be less energy recovery with such signals. Even overlapping clock signals could be used, although the circuitry would have to be different.

Although having illustrated only one segment of digital logic, digital logic **109**, the clock-powered logic shown in FIG. 8 is often repeated, much like the architecture that is shown in FIG. 1. FIG. 8 is intended to merely illustrate the overall topology of a section of the typical clock-powered logic system that incorporates the invention.

FIG. 9 is a circuit of one embodiment of the invention shown in FIG. 8.

The clocked buffer **101** can be the same circuit as was discussed above in connection with the clocked buffer of the prior art, such as the circuitry shown in FIG. 4. As will soon be seen, however, the invention does not require a "hot clock." Thus, the magnitude of the voltage of ϕ_B (as well as ϕ_A , as will be seen later) can be below the supply voltage. This is accomplished with an appropriate reduction in V_{iso} (see FIG. 4), as should be readily apparent to the skilled artisan.

A capacitor **121** reflects the capacitance that is exhibited by the signal line **120** over which the clocked signal from the clocked buffer **101** is delivered. The signal line

120 is usually long with respect to the distances between the circuitry components in the digital logic 109; however, this is not a requirement of the invention.

The level booster 103 and the latch 105 in FIG. 8 are implemented in FIG. 9 by a single jam latch 123. As should be obvious to those skilled in the art, the jam latch 123 is set by a rising edge from the clocked buffer 101 and reset by a rising edge from the clock signal ϕ_A . As is known, a jam latch is an example of a device that converts a pulse to a level and also boosts the level of the signal. Other devices that perform one or more of these functions could also be used, albeit with varying results.

The output of the jam latch 123 is then delivered to an n-latch 125 that implements the latch 107 shown in FIG. 8. The n-latch is set by a rising edge from the output of the jam latch 123 and reset by a rising edge from the clock signal ϕ_B . As is known, an n-latch is an example of a device that can be clocked by a small-swing signal. Other devices that perform this function could be used instead.

The output of the n-latch 125 is then delivered to the digital logic 109, which is the same as the digital logic 109 shown in FIG. 8. The output of the digital logic 109 is then delivered to a second n-latch 127 that preserves the output of the digital logic 109 under the control of the clock signal ϕ_A . The output of the n-latch 127 is then delivered as the output data, D_{out} .

The advantages of this configuration over the prior art configuration shown in FIG. 1 should now be apparent. First, the level boosting function of the jam latch 123 allows the system to function with a low clock signal voltage. Second, the use of two latches, the jam latch 123 and the n-latch 125, prolongs the period during which the clocked data signal is delivered to the digital logic 109 for almost a complete clock signal cycle, thereby giving the digital logic 109 far more time to develop the necessary output before the input signal is removed. Further, all of these functions are also achieved with a clock signal voltage that is below the supply voltage.

FIG. 10 is a block diagram of another embodiment of the invention using complementary input signals, but only a single latch between the clocked buffer and the digital logic. As shown in FIG. 10, a complementary clocked buffer 141 receives complementary data signals and, under the control of clock signal ϕ_B , delivers complementary clocked buffer outputs to a complementary level booster 143. In turn, the output of the complementary level booster 143 is delivered to a complementary latch

145. The output of the complementary latch 145 is delivered to complementary digital logic 147. The output of the complementary digital logic 147 is delivered to a complementary latch 149. The output of the complementary latch is a complementary set of D_{out} . The complementary latch 149 is operated under the control of clock signal ϕ_A .

5 The use of these complementary signals enables the embodiment of FIG. 10 to essentially achieve all of the advantages and benefits of the embodiment of FIG. 8, without the second latch 107 that is shown in FIG. 8. Unlike the embodiment in FIG. 8, the first latch 145 in FIG. 10 is reset by the complementary clocked and boosted signal, as opposed to being reset by ϕ_A , as is the first latch 105 in FIG. 8.

10 FIG. 11 is a circuit of one embodiment of the level booster 143 and the latch 145 that is shown in FIG. 10. As can be seen in FIG. 11, the complementary output of the clocked buffer 141 is used to control a jam latch 151 that is included as a component. Because the jam latch 151 is no longer reset by the clock signal ϕ_A , as it was in FIG. 9, the output of the latch intrinsically remains high throughout the clock signal period, thus
15 giving the digital logic 147 more time for processing, without the addition of a second latch, such as the latch 107 shown in FIG. 8.

FIG. 12 is a block diagram of a still further embodiment of the invention that does not use two latches between the clocked buffer and the digital logic, nor complementary data signals. This configuration is essentially the same as the one shown in FIG. 8, except
20 that the second latch 107 is missing. With this configuration, the digital logic 109 is not given more time to process the input signal than it was given in the prior art circuit shown in FIG. 1. On the other hand, the system of FIG. 12 still eliminates the need for "hot clocks."

25 The embodiments of the invention that thus-far been described are for illustration purposes only. The invention is not limited to these embodiments. Rather, the invention encompasses a broad variety of other embodiments and signal processing approaches and is limited solely by the claims that now follow.

CLAIMS

1. A digital system for receiving an input digital signal and for generating an
2 output digital signal that is related to the input digital signal comprising:
 - 4 a) a signal level booster having an input configured to be in
communication with a signal that is reflective of the input digital signal
and an output that is reflective of the input to said signal level booster,
6 but of greater magnitude;
 - 8 b) a first latch having an input in communication with the output of said
signal level booster, configured to be toggled by the output of said
signal level booster and by a first clock signal, and having an output;
 - 10 c) digital logic having an input in communication with a signal that is
reflective of the output of said first latch and having an output; and
 - 12 d) a second latch having an input in communication with the output of said
digital logic, configured to be toggled by the output of said digital logic
and by the first clock signal, and having an output configured to deliver
14 the output digital signal.
2. The digital system of claim 1 in which a jam latch functions as said signal
2 level booster and said first latch.
3. The digital system of claim 2 in which said second latch includes an n-latch.
4. The digital system of claim 1 in which said second latch includes an n-latch.
5. The digital system of claim 1 in which the input digital signal and the output
2 digital signal are each a single signal.
6. The digital system of claim 1 in which the input digital signal and the output
2 digital signal are each a complementary pair of signals.
7. The digital system of claim 1 further including a clocked buffer configured
2 to be powered by a second clock signal that is complementary to and substantially non-
overlapping with the first clock signal and having an input configured to be in
4 communication with the input digital signal and having an output in communication with
said signal level booster.

2 8. The digital system of claim 7 in which the second clock signal is an adiabatic signal.

9. The digital system of claim 8 in which the adiabatic signal includes blips.

2 10. The digital system of claim 8 in which the adiabatic signal includes a staircase signal.

2 11. The digital system of claim 8 in which the adiabatic signal includes a ramp signal.

2 12. The digital system of claim 8 in which the input digital signal is a complementary pair of signals and in which the input to said clocked buffer is configured to be in communication with the complementary pair of signals.

2 13. The digital system of claim 8 further including a third latch having an input in communication with the output of said first latch, configured to be toggled by the output of said first latch and by the second clock signal, and having an output in 4 communication with the input to said digital logic.

14. The digital system of claim 13 in which said third latch includes an n-latch.

2 15. The digital system of claim 14 in which said jam latch functions as said signal level booster and said first latch.

2 16. The digital system of claim 15 in which said second latch includes an n-latch.

2 17. A method for generating an output digital signal that is related to an input digital signal comprising:

- a) boosting an incoming signal that is reflective of the input digital signal;
- 4 b) latching the boosted signal under the control of a first clock signal;
- c) processing a pre-processed signal that is reflective of the latched signal 6 with digital logic;
- d) latching the processed signal under the control of the first clock; and
- 8 e) delivering the latched processed signal as the output digital signal.

2 18. The method of claim 17 in which the input digital signal and the output digital signal are each a single signal.

19. The method of claim 17 in which the input digital signal and the output.
2 digital signal are each a complementary pair of signals.

20. The method of claim 17 further including clocking the input digital signal
2 under the power of a second clock signal that is complementary to and substantially non-
overlapping with the first clock signal and delivering this clocked signal as the incoming
4 signal.

21. The method of claim 20 in which the second clock signal is an adiabatic
2 signal.

22. The method of claim 21 in which the adiabatic signal includes blips.

23. The method of claim 21 in which the adiabatic signal includes a staircase
2 signal.

24. The method of claim 21 in which the adiabatic signal includes a ramp
2 signal.

25. The method of claim 21 in which the input digital signal is a
2 complementary pair of signals and in which the clocked signal is based on the
complementary pair of signals.

26. The method of claim 21 further including latching the latched signal under
2 the control of the second clock signal and delivering that twice latched signal as the pre-
processed signal.

27. A digital system comprising:
2 a) a clocked buffer;
b) a signal line having two ends, one end of which is in communication
4 with said clocked buffer;
c) a jam latch in communication with the other end of said signal line;
6 d) digital logic in communication with said jam latch; and
e) a first n-latch in communication with said digital logic.

28. The digital system of claim 27 further including a second n-latch in
2 communication with said jam latch and said digital logic.

29. The digital system of claim 28 wherein:

- 2 a) said jam latch and said first n-latch are controlled by a first clock signal;
and
4 b) said clocked buffer and said second n-latch are controlled by a second
clock signal that is complementary to and substantially non-overlapping
6 with the first clock signal.

30. A clock-powered logic system containing logic configured to be connected
2 to a supply voltage and configured to be powered by at least one clock having a voltage
of a magnitude that does not exceed the magnitude of the supply voltage.

31. The clock-powered logic system of claim 30 in which said logic is
2 configured to be powered by at least one clock having a voltage of a magnitude that is
less than the magnitude of the supply voltage.

32. The clock-powered logic system of claim 30 in which said system includes
2 a jam latch.

33. The clock-powered logic system of claim 30 in which said system includes
2 a level booster circuit.

34. The clock-powered logic system of claim 30 in which said system includes
2 a pulse-to- level converter.

35. The clock-powered logic system of claim 30 in which said system includes
2 an n-latch.

36. The clock-powered logic system of claim 30 in which said system includes
2 a device that can be clocked by a signal of smaller magnitude than the supply voltage.

37. The clock-powered logic system of claim 30 in which said system includes
2 a clocked buffer.

38. The clock-powered logic system of claim 30 in which said system is
2 configured to utilize an adiabatic signal.

39. The clock-powered logic system of claim 38 in which the adiabatic signal
2 includes blips.

40. The clock-powered logic system of claim 38 in which the adiabatic signal
2 includes a staircase signal.

41. The clock-powered logic system of claim 38 in which the adiabatic signal
2 includes a ramp signal.

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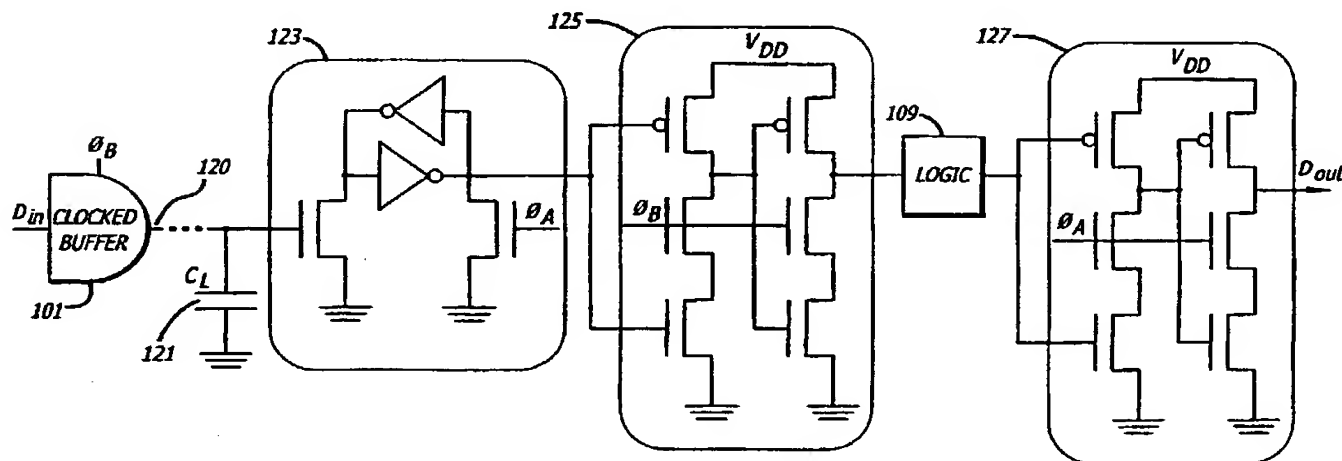
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(54) Title: **HIGH-PERFORMANCE CLOCK-POWERED LOGIC**



(57) Abstract: High performance clock-powered logic runs at below supply levels and reduces the need for faster digital logic circuitry. In a preferred embodiment, a clocked buffer (101) is used to drive the signal line. The receiving end of the line is connected to a jam latch (123), preferably followed by an n-latch (125), followed by the digital logic (109), and followed by a second n-latch (127). The first n-latch is eliminated in an alternative embodiment, preferably one that uses complementary data signals.

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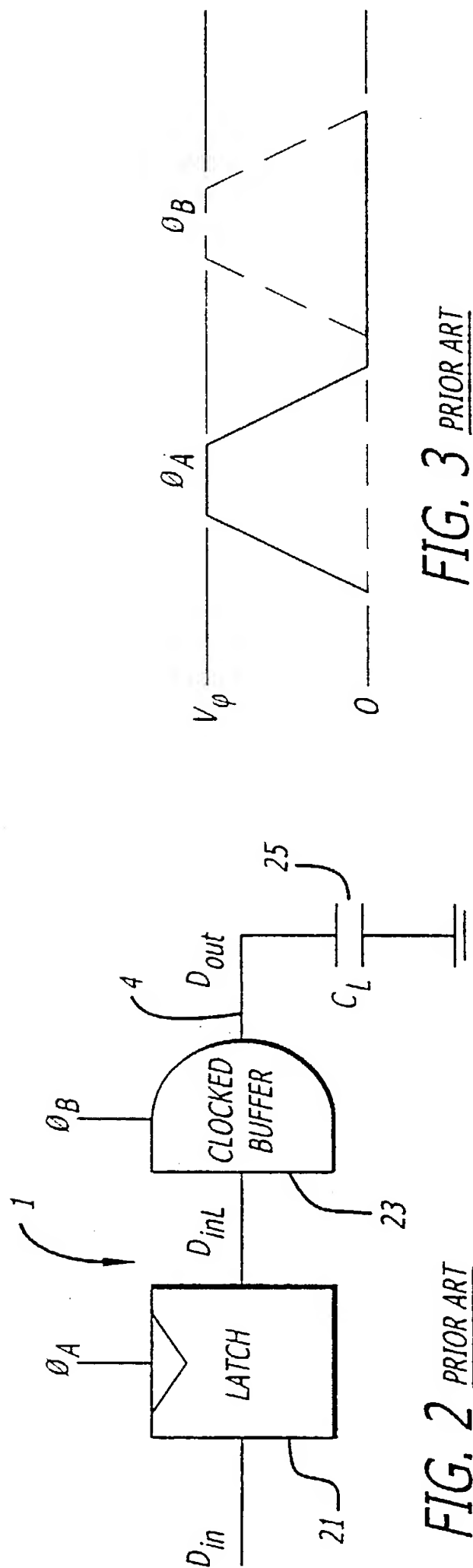
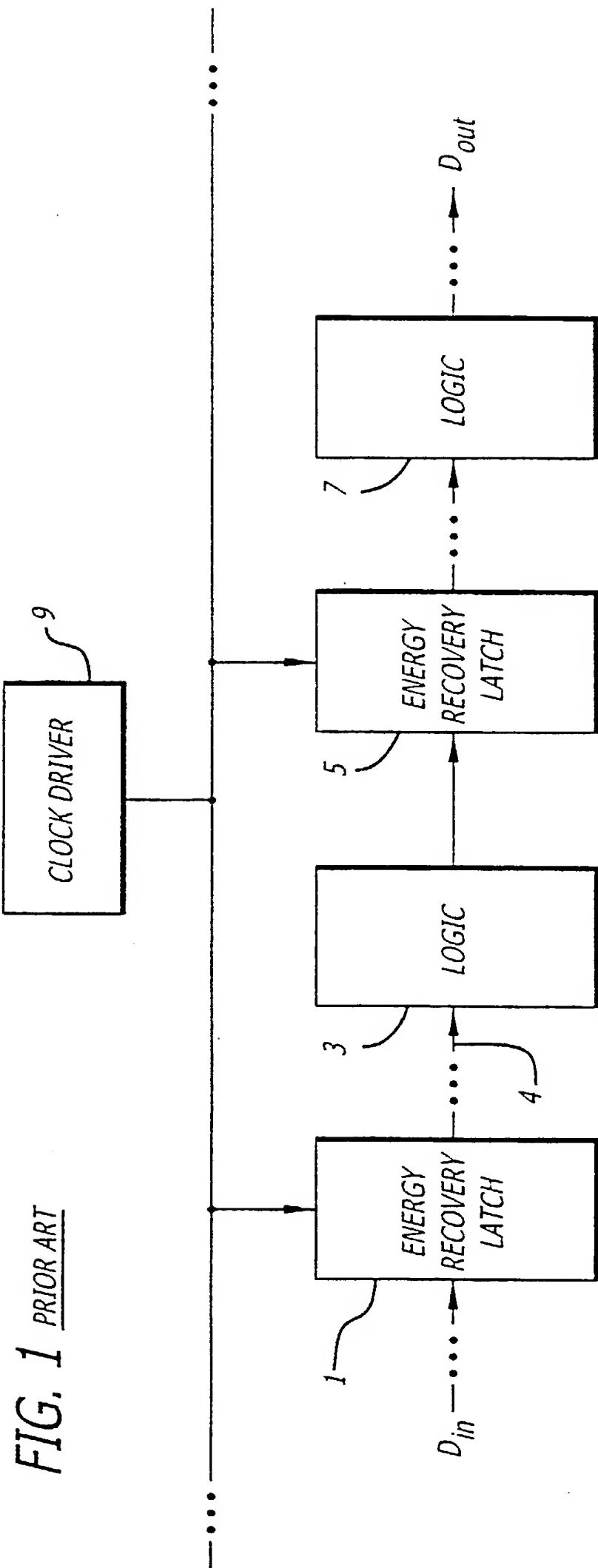
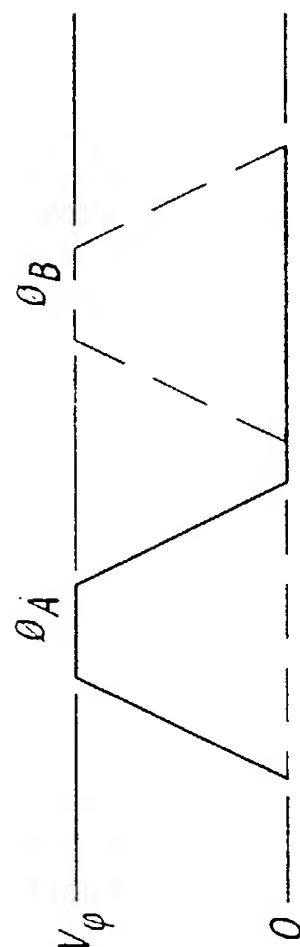


FIG. 3 PRIOR ART



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FIG. 4 PRIOR ART

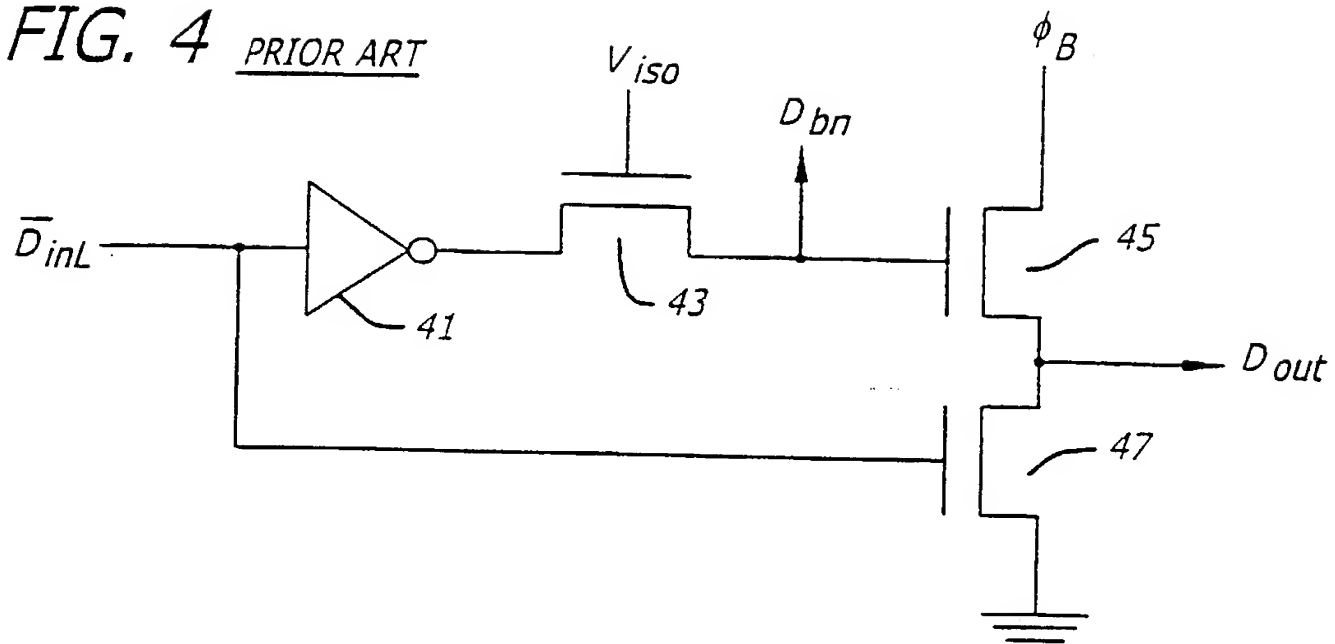


FIG. 5 PRIOR ART

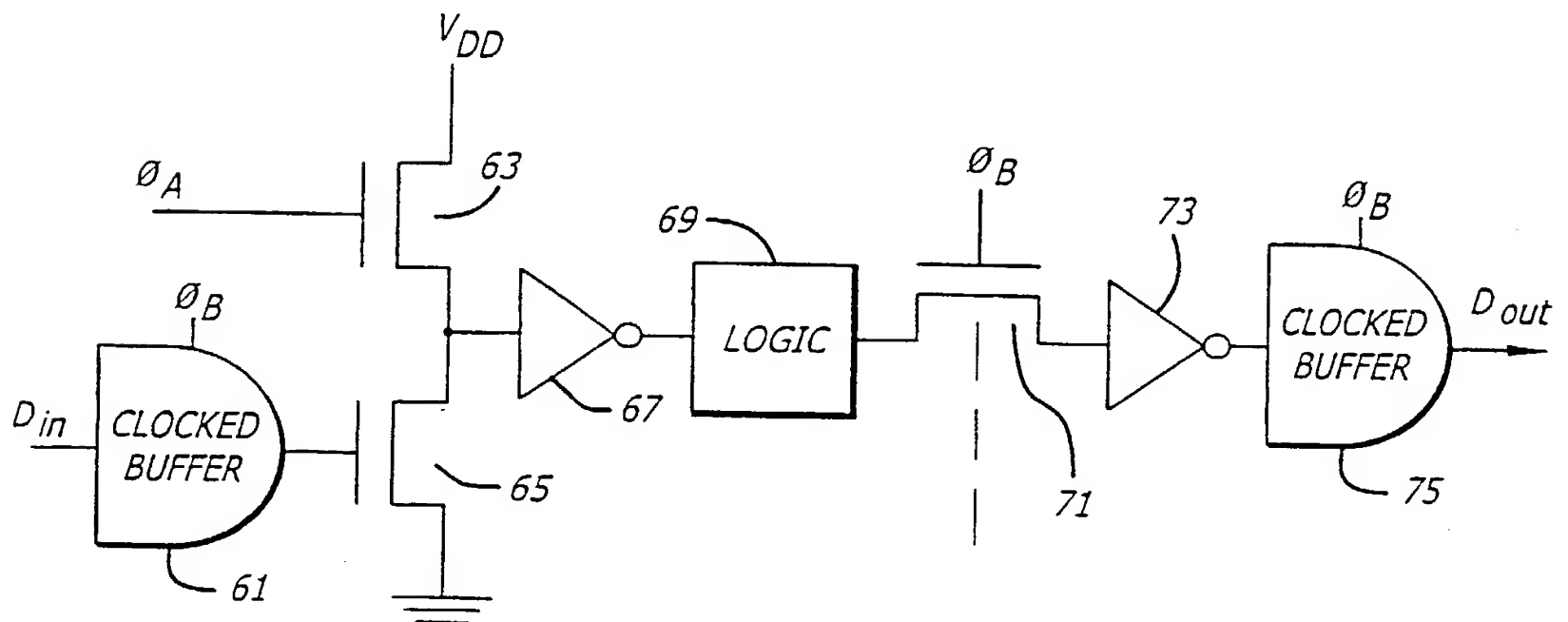
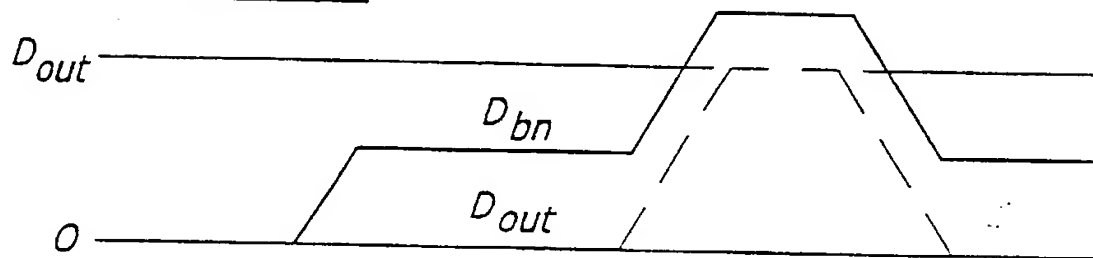
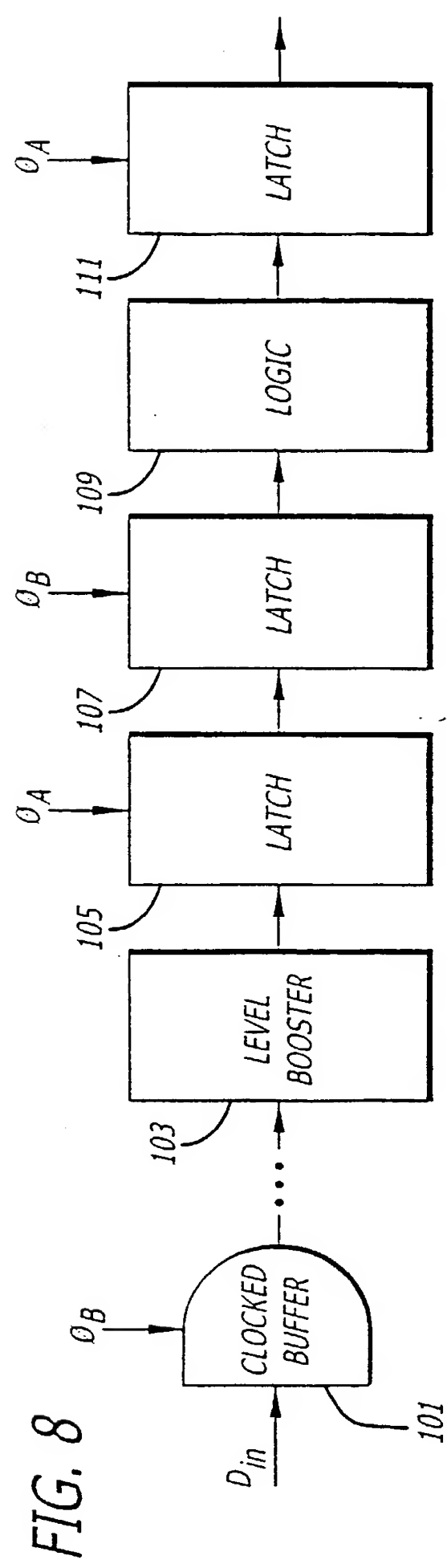
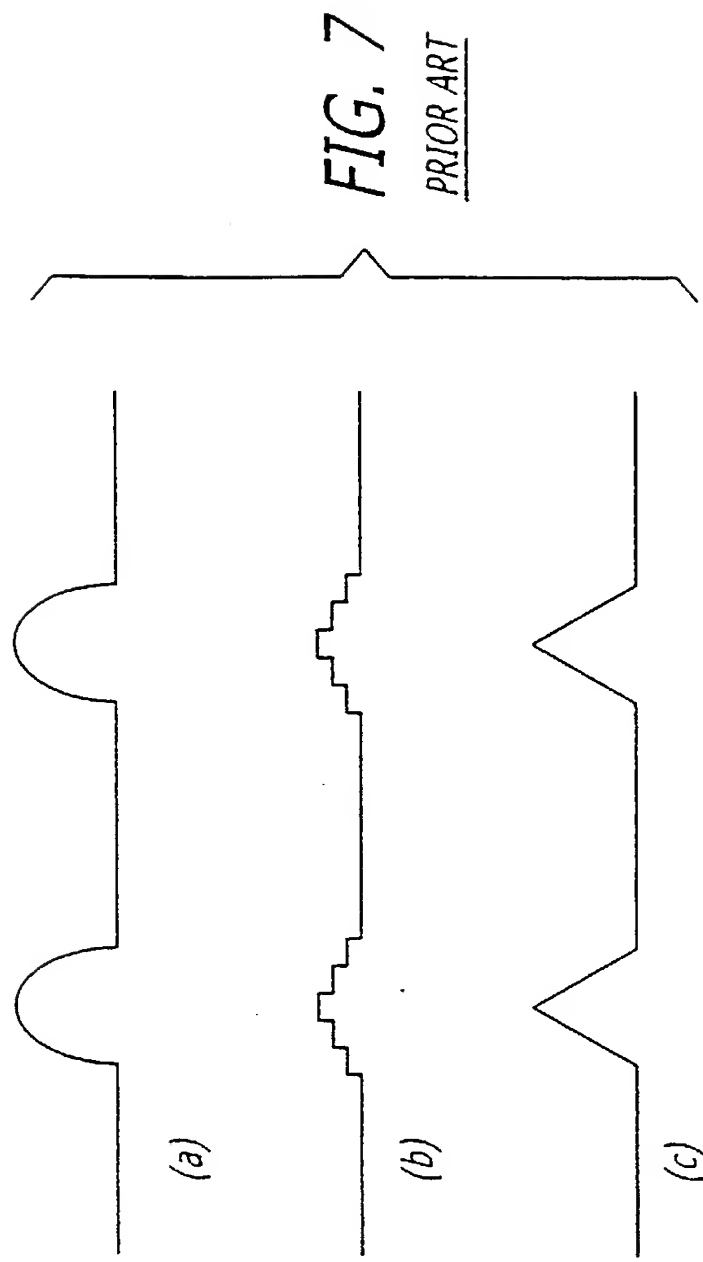
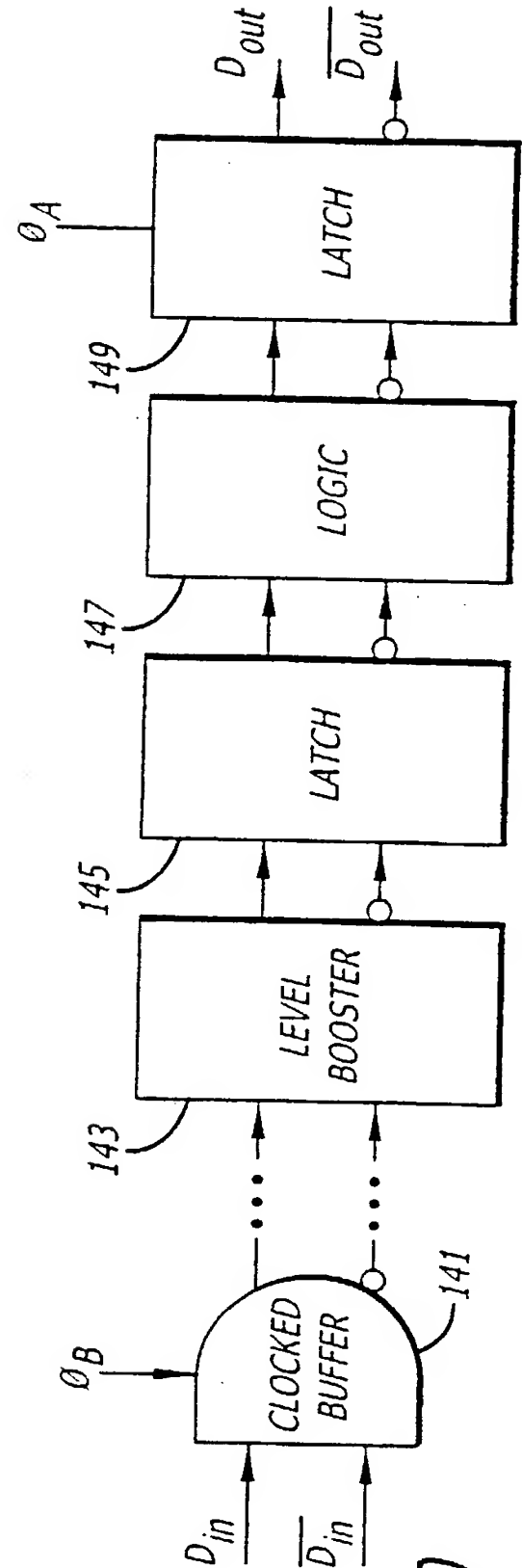
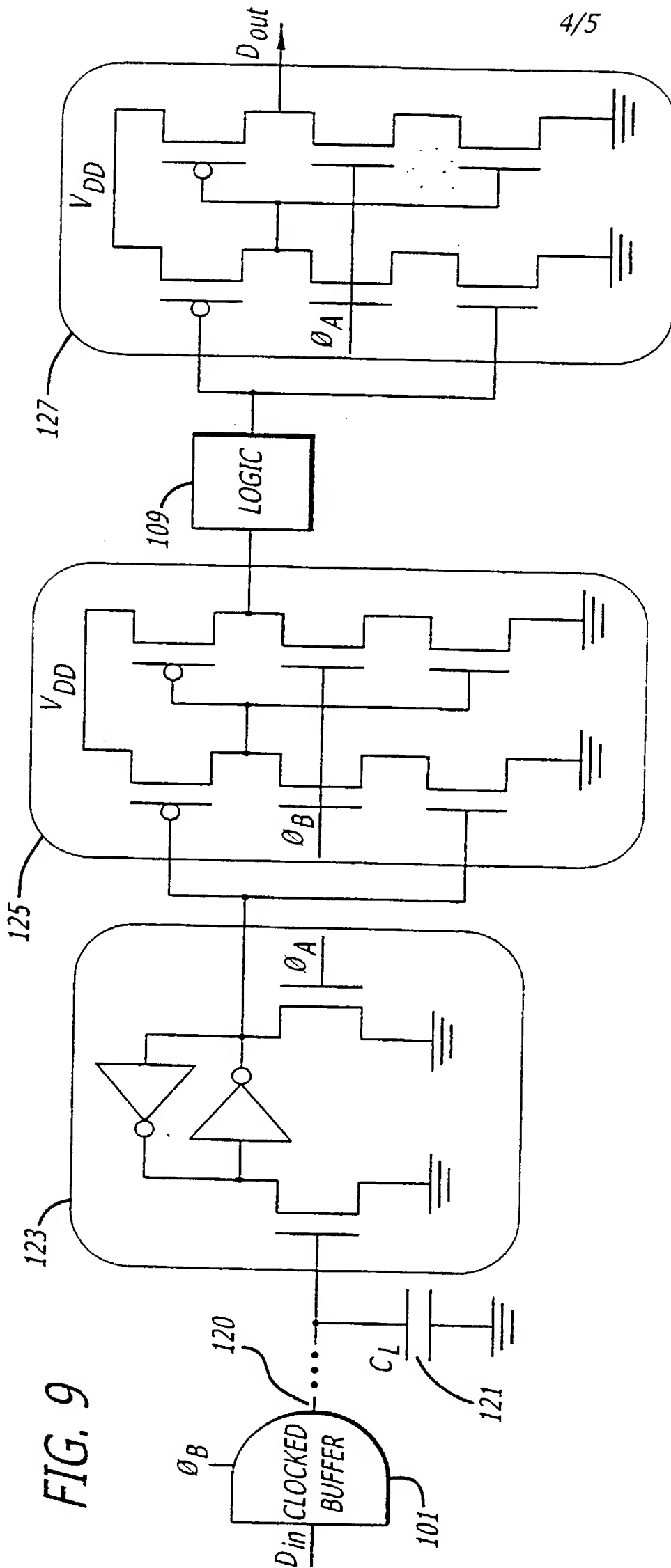
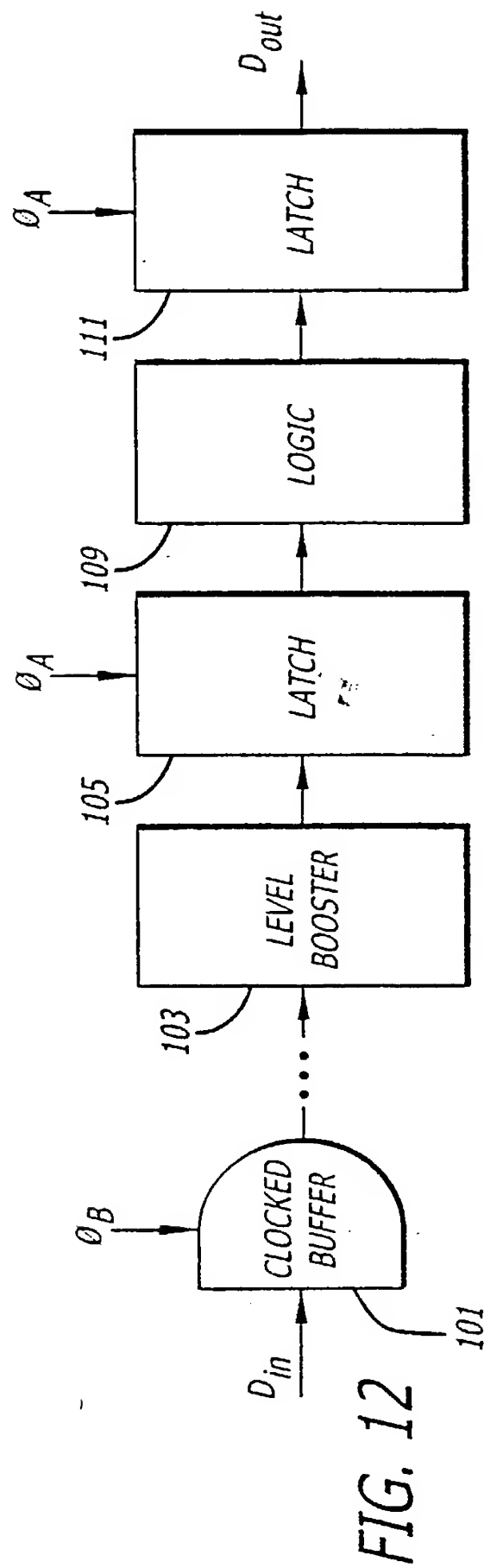
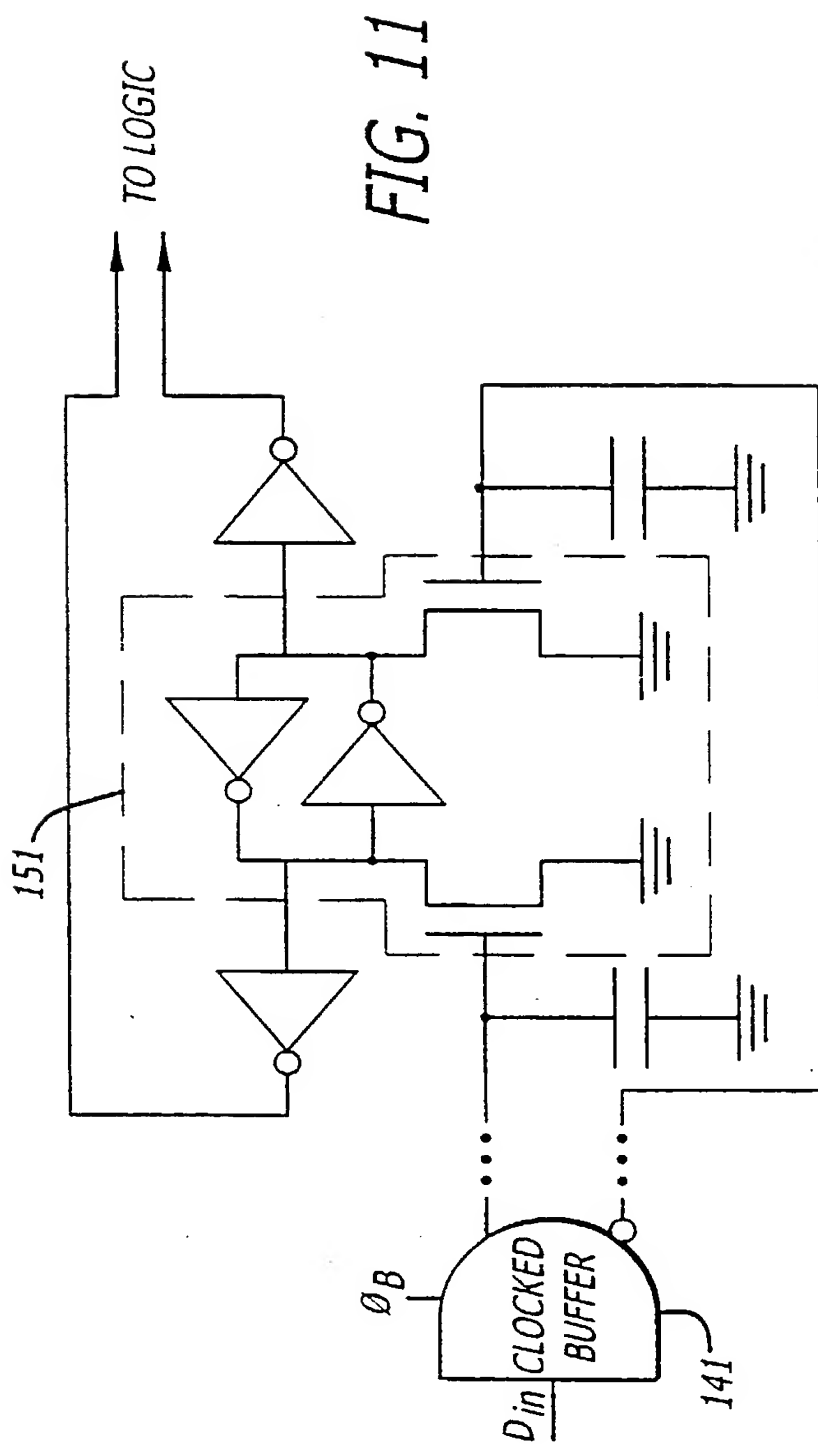


FIG. 6 PRIOR ART









10031672.090902

Docket No. 18036-24199

DECLARATION AND PETITION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled HIGH PERFORMANCE CLOCK-POWERED LOGIC, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. § 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application of which priority is claimed.

PRIOR FOREIGN APPLICATION(S)

Number	Country	Filing Date	Priority Claimed?
PCT/US00/19608	PCT	18 July 2000	Yes

PRIOR UNITED STATES APPLICATION(S)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status
60/144,520	19 July 1999	Provisional
60/174,509	5 January 2000	Provisional

I hereby declare: All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Wherefore I pray that Letters Patent be granted to me for the invention or discovery described and claimed in the foregoing specification and claims, and I hereby subscribe my name to the foregoing specification and claims, declaration, power of attorney, and this petition.

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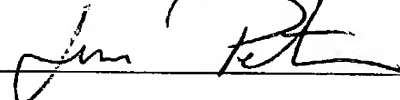
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